# XILINX® Class Schedule by Location

Important Notice:

1. Class Schedule list below is as of December 06, 2018.
2. Class dates are subject to change due to low enrollment. Please contact your local training representative if you have any questions.
3. Confirm any timezone diffrences with the ATP when you register.

If you have any questions, please contact the Registrar at registrar@xilinx.com.

## United States Texas- Richardson

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 1/15/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1600 (USD) | 16 | Register |
| **Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 1/17/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1600 (USD) | 16 | Register |
| **Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 2/26/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1400 (USD) | 14 | Register |
| **Zynq UltraScale+ MPSoC for the Software Developer** | | | | | |
| 2/28/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1600 (USD) | 16 | Register |
| **Classroom - Designing with VHDL** | | | | | |
| 2/19/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 2400 (USD) | 24 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 3/19/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1600 (USD) | 16 | Register |
| **Classroom - UltraFast Design Methodology** | | | | | |
| 1/22/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1600 (USD) | 16 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 1/24/2019 | 3101 E. Pres George Bush Richardson | USA, TX, Richardson - Avnet Office | 1600 (USD) | 16 | Register |

## United States NewYork- Hauppauge

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 12/12/2018 | 135 Engineers Rd Hauppauge | USA, NY, Hauppauge - Avnet Office | 2400 (USD) | 24 | Register |
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 1/30/2019 | 135 Engineers Rd Hauppauge | USA, NY, Hauppauge - Avnet Office | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-3 (BLT version)** | | | | | |
| 3/13/2019 | 135 Engineers Rd Hauppauge | USA, NY, Hauppauge - Avnet Office | 2700 (USD) | 27 | Register |
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 3/20/2019 | 135 Engineers Rd Hauppauge | USA, NY, Hauppauge - Avnet Office | 3000 (USD) | 30 | Register |

## United States NewJersey- Marlton

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Boot Camp Phase-1 (BLT version)** | | | | | |
| 1/23/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 2700 (USD) | 27 | Register |
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 1/28/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 3000 (USD) | 30 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 2/18/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 1600 (USD) | 18 | Register |
| **Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 2/20/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 1000 (USD) | 10 | Register |
| **DSP Design Using System Generator** | | | | | |
| 2/21/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 2000 (USD) | 20 | Register |
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 3/18/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-3 (BLT version)** | | | | | |
| 4/29/2019 | 13000 Lincoln Drive West Marlton | USA, NJ, Marlton - Avnet Office | 2700 (USD) | 27 | Register |

## United States NewYork- Rochester

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 1/23/2019 | 245 Kenneth Drive Rochester | USA, NY, Rochester - Avnet Office | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-3 (BLT version)** | | | | | |
| 3/6/2019 | 245 Kenneth Drive Rochester | USA, NY, Rochester - Avnet Office | 2700 (USD) | 27 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 3/25/2019 | 245 Kenneth Drive Rochester | USA, NY, Rochester - Avnet Office | 1800 (USD) | 18 | Register |
| **Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 3/27/2019 | 245 Kenneth Drive Rochester | USA, NY, Rochester - Avnet Office | 1000 (USD) | 10 | Register |
| **DSP Design Using System Generator** | | | | | |
| 3/28/2019 | 245 Kenneth Drive Rochester | USA, NY, Rochester - Avnet Office | 2000 (USD) | 20 | Register |
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 4/10/2019 | 245 Kenneth Drive Rochester | USA, NY, Rochester - Avnet Office | 3000 (USD) | 30 | Register |

# The Netherlands - Heesch

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing with the UltraScale and UltraScale+ Architectures** | | | | | |
| 12/20/2018 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users** | | | | | |
| 1/9/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Zynq UltraScale+ MPSoC for the Hardware Designer** | | | | | |
| 1/18/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 750 (EUR) | 9 | Register |
| **Classroom - Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 1/16/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 1/28/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Designing with Xilinx Serial Transceivers** | | | | | |
| 1/23/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - SDSoC Development Environment and Methodology** | | | | | |
| 1/30/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 750 (EUR) | 9 | Register |
| **Classroom - Advanced SDSoC Development Environment and Methodology** | | | | | |
| 1/31/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 2/4/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1600 (EUR) | 18 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 2/6/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Essential Digital Design Techniques (CoreVision Version)** | | | | | |
| 12/18/2018 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1695 (EUR) | 27 | Register |
| **Classroom - Comprehensive VHDL (CoreVision Version)** | | | | | |
| 12/10/2018 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 3695 (EUR) | 58 | Register |
| **Classroom - VHDL for Designers (CoreVision Version)** | | | | | |
| 12/10/2018 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 2595 (EUR) | 41 | Register |
| **Classroom - Advanced VHDL (CoreVision Version)** | | | | | |
| 12/13/2018 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1795 (EUR) | 28 | Register |
| **Classroom - Designing with the UltraScale and UltraScale+ Architectures** | | | | | |
| 2/13/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Embedded Systems Design** | | | | | |
| 2/18/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Embedded Systems Software Design** | | | | | |
| 2/20/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Expert VHDL (CoreVision Version)** | | | | | |
| 2/25/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 3795 (EUR) | 59 | Register |
| **Classroom - Expert VHDL Verification (CoreVision Version)** | | | | | |
| 2/27/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 2595 (EUR) | 41 | Register |
| **Classroom - Zynq SoC System Architecture** | | | | | |
| 3/4/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Advanced Features and Techniques of Embedded Systems Design** | | | | | |
| 3/6/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |
| **Classroom - Advanced Features and Techniques of Embedded Systems Software Design** | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| 3/8/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 750 (EUR) | 9 | Register |

### Classroom - Comprehensive VHDL (CoreVision Version)

| | | | | | |
|---|---|---|---|---|---|
| 3/11/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 3795 (EUR) | 59 | Register |

### Classroom - VHDL for Designers (CoreVision Version)

| | | | | | |
|---|---|---|---|---|---|
| 3/11/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 2695 (EUR) | 42 | Register |

### Classroom - Advanced VHDL (CoreVision Version)

| | | | | | |
|---|---|---|---|---|---|
| 3/14/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1795 (EUR) | 28 | Register |

### Classroom - Designing FPGAs Using the Vivado Design Suite 3

| | | | | | |
|---|---|---|---|---|---|
| 3/18/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - Designing FPGAs Using the Vivado Design Suite 4

| | | | | | |
|---|---|---|---|---|---|
| 3/20/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - UltraFast Design Methodology

| | | | | | |
|---|---|---|---|---|---|
| 3/28/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - Essential Digital Design Techniques (CoreVision Version)

| | | | | | |
|---|---|---|---|---|---|
| 3/25/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1795 (EUR) | 28 | Register |

### Classroom - C-based design: High-Level Synthesis with Vivado HLx Tool

| | | | | | |
|---|---|---|---|---|---|
| 4/1/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - SDSoC Development Environment and Methodology

| | | | | | |
|---|---|---|---|---|---|
| 4/3/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 750 (EUR) | 9 | Register |

### Classroom - Advanced SDSoC Development Environment and Methodology

| | | | | | |
|---|---|---|---|---|---|
| 4/4/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - DSP Design Using System Generator

| | | | | | |
|---|---|---|---|---|---|
| 4/11/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - Essential DSP Implementation Techniques for Xilinx FPGAs

| | | | | | |
|---|---|---|---|---|---|
| 4/18/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - Zynq UltraScale+ MPSoC for the System Architect

| | | | | | |
|---|---|---|---|---|---|
| 4/24/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 1500 (EUR) | 18 | Register |

### Classroom - Zynq UltraScale+ MPSoC for the Hardware Designer

| | | | | | |
|---|---|---|---|---|---|
| 4/26/2019 | Cereslaan 10b Heesch | NLD, Heesch - CoreVision Headquarters | 750 (EUR) | 9 | Register |

## United Kingdom - Ringwood

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|

### ARM Cortex-A53 for Zynq UltraScale+ MPSoC (Doulos course)

| | | | | | |
|---|---|---|---|---|---|
| 12/10/2018 | Doulos Ltd, Church Hatch, 22 Market Place Ringwood | GBR, Ringwood - Doulos Headquarters | 3100 (GBP) | 36 | Register |

### Comprehensive VHDL (Doulos version)

| | | | | | |
|---|---|---|---|---|---|
| 12/10/2018 | Doulos Ltd, Church Hatch, 22 Market Place Ringwood | GBR, Ringwood - Doulos Headquarters | 2995 (GBP) | 45 | Register |

### Virtual - SDSoC Adopter Class (Doulos version)

| | | | | | |
|---|---|---|---|---|---|
| 1/30/2019 | Doulos Ltd, Church Hatch, 22 Market Place Ringwood | GBR, Ringwood - Doulos Headquarters | 2400 (GBP) | 27 | Register |

### Classroom - Vivado Adopter Class (Doulos version)

| | | | | | |
|---|---|---|---|---|---|
| 1/22/2019 | Doulos Ltd, Church Hatch, 22 Market Place Ringwood | GBR, Ringwood - Doulos Headquarters | 3100 (GBP) | 36 | Register |

## Taiwan - Taipei

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing with the UltraScale and UltraScale+ Architectures** | | | | | |
| 12/13/2018 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 20000 (USD) | 16 | Register |
| **Designing with Ethernet MAC Controllers** | | | | | |
| 12/20/2018 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 12/27/2018 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 1/24/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 1/15/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 20000 (USD) | 16 | Register |
| **Embedded Systems Design** | | | | | |
| 1/10/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Designing with UltraScale FPGA Transceivers** | | | | | |
| 1/29/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 2/14/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 2/21/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 16 | Register |
| **Introduction to Zynq All Programmable SoC Architecture** | | | | | |
| 2/26/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 20000 (USD) | 6 | Register |
| **Designing an Integrated PCI Express System** | | | | | |
| 3/7/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 6 | Register |
| **Embedded Systems Design** | | | | | |
| 3/12/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 6 | Register |
| **Designing with the UltraScale and UltraScale+ Architectures** | | | | | |
| 3/14/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 6 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 3/19/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 6 | Register |
| **Designing with Ethernet MAC Controllers** | | | | | |
| 3/26/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 6 | Register |
| **Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 3/28/2019 | 5F, No.61, Lane76, Ruiguang Rd. Taipei | TWN, Taipei - E-Elemements Office | 1600 (USD) | 6 | Register |

## United States Massachusetts- Burlington

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Accelerating C C++ OpenCL & RTL Applications w SDAccel - Classroom** | | | | | |
| 2/14/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 1800 (USD) | 18 | Register |
| **Developing AWS F1 Applications Using the SDAccel Environment Course - Classroom** | | | | | |
| 2/11/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 900 (USD) | 9 | Register |

## Canada Quebec- Montreal

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **SDSoC Development Environment and Methodology** | | | | | |
| 12/19/2018 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 800 (USD) | 8 | Register |
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 1/21/2019 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 2400 (USD) | 24 | Register |
| **Embedded System Design for the Zynq UltraScale+ MPSoC (combined course)** | | | | | |
| 3/6/2019 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 2400 (USD) | 24 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 1/24/2019 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 1600 (USD) | 16 | Register |
| **Introduction to Universal Verification Methodology (UVM)** | | | | | |
| 1/21/2019 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 2800 (USD) | 28 | Register |
| **Embedded Design with PetaLinux Tools** | | | | | |
| 3/4/2019 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 1600 (USD) | 16 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 12/20/2018 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 1600 (USD) | 16 | Register |
| **Accelerating C C++ OpenCL & RTL Applications w SDAccel - Classroom** | | | | | |
| 1/14/2019 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 1800 (USD) | 18 | Register |
| **Developing AWS F1 Applications Using the SDAccel Environment Course - Classroom** | | | | | |
| 12/20/2018 | 450 Saint Pierre, #300 Montreal | CAN, QC, Montreal - Hardent Headquarters | 900 (USD) | 9 | Register |

## Japan - Yokohama

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **RTL(Verilog) Design with Vivado Design Suite (HDLab version)** | | | | | |
| 1/8/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 113510 (JPY) | 8 | Register |
| **Classroom - UltraFast Design Methodology** | | | | | |
| 1/24/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 1600 (JPY) | 8 | Register |
| **Understand Simulation with Vivado Design Suite (HDLab version)** | | | | | |
| 2/12/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 45404 (JPY) | 4 | Register |
| **Vivado Design Suite Static Constraints and Timing Analysis (HDLab version)** | | | | | |
| 2/13/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 45404 (JPY) | 4 | Register |
| **RTL(Verilog) Design with Vivado Design Suite (HDLab version)** | | | | | |
| 2/19/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 113510 (JPY) | 8 | Register |
| **Vivado Design Suite Static Timing Closure (HDLab version)** | | | | | |
| 2/28/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 45404 (JPY) | 4 | Register |
| **MicroBlaze for beginner with ARTY Board ( HDLab course)** | | | | | |
| 3/7/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 45404 (JPY) | 4 | Register |
| **Vivado Design Suite Tool Flow with Artix-7 Board (HDLab course)** | | | | | |
| 3/8/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 45404 (JPY) | 4 | Register |
| **RTL(VHDL) Design with Vivado Design Suite (HDLab version)** | | | | | |
| 3/11/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 113510 (JPY) | 8 | Register |
| **C for beginner with Vivado HLS tool (HDLab version)** | | | | | |
| 3/18/2019 | Innotec Bldg 10F 3-17-6, Shin-Yokohama, Kouhoku-ku Yokohama | JPN, Yokohama - HDLab Headquarters | 45404 (JPY) | 4 | Register |

## United States California- El Segundo

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 12/17/2018 | 2100 East Mariposa Ave El Segundo | USA, CA, El Segundo - Hilton Garden Inn | 1600 (USD) | 16 | Register |

## Israel - Petah-Tikva

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Design Suite Advanced XDC and Timing Analysis for ISE Users** | | | | | |
| 12/26/2018 | 32 Shacham St, Ramat-Siv Industrial Park Petah-Tikva | ISR, Petah-Tikva - Logtel Headquarters | 1600 (USD) | 15 | Register |
| **PCIe Gen1.X to 4.X (Logtel course)** | | | | | |
| 12/24/2018 | 32 Shacham St, Ramat-Siv Industrial Park Petah-Tikva | ISR, Petah-Tikva - Logtel Headquarters | 7096 (USD) | 15 | Register |
| **Advanced Designing with Verilog (Logtel version)** | | | | | |
| 12/11/2018 | 32 Shacham St, Ramat-Siv Industrial Park Petah-Tikva | ISR, Petah-Tikva - Logtel Headquarters | 3548 (USD) | 10 | Register |
| **Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 12/10/2018 | 32 Shacham St, Ramat-Siv Industrial Park Petah-Tikva | ISR, Petah-Tikva - Logtel Headquarters | 1600 (USD) | 15 | Register |

## Russia - Moscow

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Classroom - Designing with VHDL** | | | | | |
| 12/17/2018 | 78, prospect Vernadskogo Moscow | RUS, Moscow - MIREA | 1500 (RUB) | 15 | Register |
| **Classroom - Designing with SystemVerilog** | | | | | |
| 12/10/2018 | 78, prospect Vernadskogo Moscow | RUS, Moscow - MIREA | 1600 (RUB) | 16 | Register |

## France - Sèvres

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 12/11/2018 | 7 avenue de l'europe Sèvres | FRA, Paris - MVD Training Classroom | 1600 (EUR) | 16 | Register |
| **Designing FPGAs Using the Vivado Design Suite 4** | | | | | |
| 12/13/2018 | 7 avenue de l'europe Sèvres | FRA, Paris - MVD Training Classroom | 1600 (EUR) | 16 | Register |
| **VHDL Logical Synthesis and Simulation for Xilinx? FPGA design (MVD version)** | | | | | |
| 12/17/2018 | 7 avenue de l'europe Sèvres | FRA, Paris - MVD Training Classroom | 3357 (EUR) | 40 | Register |

# Germany - Freiburg

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Professional Vivado (PLC2 version)** | | | | | |
| 12/17/2018 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 3832 (EUR) | 45 | Register |
| **Compact Advanced VHDL Testbenches and Verification /OSVVM (PLC2 course)** | | | | | |
| 12/17/2018 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 2300 (EUR) | 27 | Register |
| **Version Control for Xilinx with Git (PLC2 course)** | | | | | |
| 12/17/2018 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 2300 (EUR) | 27 | Register |
| **Tcl Schnellstart ( PLC2 version)** | | | | | |
| 12/17/2018 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 1533 (EUR) | 18 | Register |
| **Advanced Vivado Tcl-Scripting (PLC2 version)** | | | | | |
| 12/18/2018 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 2300 (EUR) | 27 | Register |
| **Professional ZYNQ-7000 SoC (PLC2 version)** | | | | | |
| 1/21/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 3100 (EUR) | 45 | Register |
| **Easy Start FPGA Vivado (PLC2 version)** | | | | | |
| 1/28/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 1700 (EUR) | 18 | Register |
| **Designing a LogiCORE PCI Express System (PLC2 version)** | | | | | |
| 5/13/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 2300 (EUR) | 27 | Register |
| **Easy Start Embedded for ZYNQ-7000 SoC Systems (PLC2 version)** | | | | | |
| 2/11/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 1533 (EUR) | 18 | Register |
| **Professional VHDL (PLC2 version)** | | | | | |
| 2/11/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 3832 (EUR) | 45 | Register |
| **Vivado Design Suite Static Timing Analysis and XILINX Design Constraints (PLC2 version)** | | | | | |
| 3/6/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 2300 (EUR) | 27 | Register |
| **Professional ZYNQ UltraScale+ MPSoC (PLC2 version)** | | | | | |
| 3/18/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 3832 (EUR) | 45 | Register |
| **Professional Vivado (PLC2 version)** | | | | | |
| 3/25/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 3832 (EUR) | 45 | Register |
| **Classroom - Designing with 7 Series** | | | | | |
| 3/14/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 1600 (EUR) | 16 | Register |
| **Professional FPGA Schaltungstechnik (PLC2 course)** | | | | | |
| 4/1/2019 | Hugstmattweg 30 Freiburg | DEU, Freiburg - PLC2 Office | 3832 (EUR) | 45 | Register |

# India - Bangalore

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **UltraFast Design Methodology** | | | | | |
| 12/10/2018 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Xilinx Partial Reconfiguration Tools & Techniques** | | | | | |
| 12/13/2018 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Zynq-7000 All Programmable SoC System Architecture** | | | | | |
| 12/17/2018 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 12/20/2018 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Designing with 7 Series** | | | | | |
| 1/3/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - Designing with the UltraScale and UltraScale+ Architectures** | | | | | |
| 1/7/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - UltraFast Design Methodology** | | | | | |
| 1/10/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Custom HLS and SDSoC** | | | | | |
| 1/17/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Custom SDAccel** | | | | | |
| 1/21/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - Designing with UltraScale FPGA Transceivers** | | | | | |
| 1/23/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Custom Partial Reconfiguration** | | | | | |
| 1/30/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 600 (USD) | 6 | Register |
| **How to Design a High-Speed Memory Interface** | | | | | |
| 2/4/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - Embedded Design with PetaLinux Tools** | | | | | |
| 2/6/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - SDSoC Development Environment and Methodology** | | | | | |
| 2/11/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 600 (USD) | 6 | Register |
| **Custom Zynq UltraScale+MPSoC** | | | | | |
| 2/13/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - Embedded Systems Software Design** | | | | | |
| 2/18/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 2/21/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 2/25/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 600 (USD) | 6 | Register |

### Classroom - Designing FPGAs Using the Vivado Design Suite 2

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| 2/27/2019 | #21, 7th Main, 1st Block, Koramangala Bangalore | IND, Bangalore - Sandeepani School of Embedded System Design | 800 (USD) | 8 | Register |

## Austria - Vienna

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 12/10/2018 | Lustkandlg. 52 Vienna | AUT, Vienna - So-Logic Office | 1500 (EUR) | 16 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx** | | | | | |
| 12/12/2018 | Lustkandlg. 52 Vienna | AUT, Vienna - So-Logic Office | 1500 (EUR) | 16 | Register |
| **DSP Design Using System Generator** | | | | | |
| 12/12/2018 | Lustkandlg. 52 Vienna | AUT, Vienna - So-Logic Office | 1500 (EUR) | 16 | Register |
| **C-based HLS Coding for Software Designers** | | | | | |
| 12/14/2018 | Lustkandlg. 52 Vienna | AUT, Vienna - So-Logic Office | 750 (EUR) | 4 | Register |
| **C-based HLS Coding for Hardware Designers** | | | | | |
| 12/14/2018 | Lustkandlg. 52 Vienna | AUT, Vienna - So-Logic Office | 750 (EUR) | 9 | Register |

## United States NewJersey- Parsippany

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Boot Camp Phase-1 (BLT version)** | | | | | |
| 1/23/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 2700 (USD) | 27 | Register |
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 1/28/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 3000 (USD) | 30 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 2/18/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 1800 (USD) | 18 | Register |
| **Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 2/20/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 1000 (USD) | 10 | Register |
| **DSP Design Using System Generator** | | | | | |
| 2/21/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 2000 (USD) | 20 | Register |
| **DSP Design Using System Generator** | | | | | |
| 3/7/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 2000 (USD) | 20 | Register |
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 3/18/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-3 (BLT version)** | | | | | |
| 4/29/2019 | 61 Interpace Parkway Parsippany | USA, NJ, Parsippany - Sonesta ES Suites | 2700 (USD) | 27 | Register |

## United States Florida- Orlando

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Embedded System Design for the Zynq UltraScale+ MPSoC (combined course)** | | | | | |
| 1/28/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **Embedded Design with PetaLinux Tools** | | | | | |
| 1/31/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 3/6/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **SystemVerilog for Verification** | | | | | |
| 3/11/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 2800 (USD) | 28 | Register |
| **Introduction to Universal Verification Methodology (UVM)** | | | | | |
| 2/4/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 2800 (USD) | 28 | Register |
| **SDSoC Development Environment and Methodology** | | | | | |
| 2/6/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 800 (USD) | 8 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 2/7/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 2/4/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 3/4/2019 | TBD Orlando | USA, FL, Orlando - TBD Hardent Venue | 1800 (USD) | 18 | Register |

## Canada Ontario- Ottawa

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 4/15/2019 | TBD Ottawa | CAN, ON, Ottawa - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 3/26/2019 | TBD Ottawa | CAN, ON, Ottawa - TBD Hardent Venue | 1800 (USD) | 18 | Register |
| **Classroom - DSP Design Using System Generator** | | | | | |
| 4/24/2019 | TBD Ottawa | CAN, ON, Ottawa - TBD Hardent Venue | 1600 (USD) | 16 | Register |

## Canada Ontario- Toronto

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Embedded System Design for the Zynq UltraScale+ MPSoC (combined course)** | | | | | |
| 1/15/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 3/11/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **SDSoC Development Environment and Methodology** | | | | | |
| 3/13/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 800 (USD) | 8 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 3/14/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **SystemVerilog for Verification (Hardent version)** | | | | | |
| 1/28/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 2800 (USD) | 28 | Register |
| **Introduction to Universal Verification Methodology (UVM) (Hardent version)** | | | | | |
| 4/8/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 2800 (USD) | 28 | Register |
| **Accelerating C C++ OpenCL & RTL Applications w SDAccel - Classroom** | | | | | |
| 1/29/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 1800 (USD) | 18 | Register |
| **Classroom - Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 5/22/2019 | TBD Toronto | CAN, ON, Toronto - TBD Hardent Venue | 2400 (USD) | 24 | Register |

## United States Indiana- TBD

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 12/7/2018 | TBD TBD | USA, IN - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Virtual - Embedded Systems Software Design** | | | | | |
| 2/18/2019 | TBD TBD | USA, IN - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 3/7/2019 | TBD TBD | USA, IN - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 3/8/2019 | TBD TBD | USA, IN - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |

## United States Ohio- TBD

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 12/13/2018 | TBD TBD | USA, OH - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Classroom - Embedded Design with PetaLinux Tools** | | | | | |
| 2/26/2019 | TBD TBD | USA, OH - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Classroom - Embedded Design with PetaLinux Tools** | | | | | |
| 2/27/2019 | TBD TBD | USA, OH - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |

## United States Michigan- TBD

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 12/12/2018 | TBD TBD | USA, MI - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Embedded Systems Design** | | | | | |
| 12/18/2018 | TBD TBD | USA, MI - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |
| **Embedded Systems Design** | | | | | |
| 12/19/2018 | TBD TBD | USA, MI - TBD VAI Logic Venue | 1600 (USD) | 16 | Register |

## Germany - Berlin

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing a LogiCORE PCI Express System (PLC2 version)** | | | | | |
| 12/10/2018 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Python (PLC2 course)** | | | | | |
| 12/10/2018 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **High-Speed Memory Interfacing (PLC2 version)** | | | | | |
| 3/11/2019 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **DDR4 Interfacing with XILINX FPGAs (PLC2 version)** | | | | | |
| 2/11/2019 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Professional PCI Express (PLC2 version)** | | | | | |
| 4/8/2019 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 3832 (EUR) | 45 | Register |
| **Easy Start FPGA Vivado (PLC2 version)** | | | | | |
| 3/18/2019 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |
| **Debugging Techniques Using the Vivado Logic Analyzer (PLC2 version)** | | | | | |
| 3/20/2019 | TBD Berlin | DEU, Berlin - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |

## Germany - Frankfurt

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Compact FPGA 7 Series (PLC2 version)** | | | | | |
| 12/10/2018 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |
| **Expert ZYNQ-7000 SoC (PLC2 version)** | | | | | |
| 12/17/2018 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 3832 (EUR) | 45 | Register |
| **FPGA Board Design (PLC2 course)** | | | | | |
| 1/24/2019 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |
| **Professional FPGA (PLC2 version)** | | | | | |
| 2/18/2019 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 3832 (EUR) | 45 | Register |
| **ZYNQ-7000 SoC System Architecture (PLC2 version)** | | | | | |
| 2/18/2019 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |
| **Compact ZYNQ UltraScale+ MPSoC for HW Designers (PLC2 version)** | | | | | |
| 2/20/2019 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Vivado Design Suite Tool Flow (PLC2 version)** | | | | | |
| 2/25/2019 | TBD Frankfurt | DEU, Frankfurt - TBD PLC2 Venue | 766 (EUR) | 9 | Register |

# Germany - Munchen

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Advanced Vivado HLS (PLC2 version)** | | | | | |
| 12/10/2018 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Compact ZYNQ UltraScale+ MPSoC for HW Designers (PLC2 version)** | | | | | |
| 12/12/2018 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **AXI Interface Technology (PLC2 version)** | | | | | |
| 12/13/2018 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |
| **Classroom - Designing with Multi-Gigabit Serial I/O** | | | | | |
| 1/28/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2200 (EUR) | 27 | Register |
| **Compact FPGA Schaltungstechnik (PLC2 course)** | | | | | |
| 1/21/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2100 (EUR) | 27 | Register |
| **Classroom - Designing with Ethernet MAC Controllers** | | | | | |
| 1/30/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 1500 (EUR) | 18 | Register |
| **UltraScale Connectivity (PLC2 version)** | | | | | |
| 3/25/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 3832 (EUR) | 45 | Register |
| **Compact Verilog (PLC2 version)** | | | | | |
| 2/11/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **DSP Design using System Generator (PLC2 version)** | | | | | |
| 2/11/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Expert DSP Design using System Generator (PLC2 version)** | | | | | |
| 2/11/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 3832 (EUR) | 45 | Register |
| **Compact ZYNQ-7000 SoC for SW Designers (PLC2 version)** | | | | | |
| 3/25/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Python (PLC2 course)** | | | | | |
| 3/25/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Compact UltraScale (PLC2 version)** | | | | | |
| 3/18/2019 | TBD Munchen | DEU, Munchen - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |

# Germany - Stuttgart

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **DDR4 Interfacing with XILINX FPGAs (PLC2 version)** | | | | | |
| 12/10/2018 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Designing a LogiCORE PCI Express System (PLC2 version)** | | | | | |
| 2/4/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Continuous Integration (PLC2 course)** | | | | | |
| 2/18/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 3832 (EUR) | 45 | Register |
| **Compact Advanced VHDL Testbenches and Verification /OSVVM (PLC2 course)** | | | | | |
| 3/6/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Classroom - Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 3/6/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 1600 (EUR) | 16 | Register |
| **Compact FPGA Schaltungstechnik (PLC2 course)** | | | | | |
| 3/20/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **Classroom - Embedded Design with PetaLinux Tools** | | | | | |
| 3/28/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 1600 (EUR) | 16 | Register |
| **Advanced Vivado HLS (PLC2 version)** | | | | | |
| 3/11/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |
| **AXI Interface Technology (PLC2 version)** | | | | | |
| 3/14/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 1533 (EUR) | 18 | Register |
| **Compact ZYNQ-7000 SoC for HW Designers (PLC2 version)** | | | | | |
| 3/13/2019 | TBD Stuttgart | DEU, Stuttgart - TBD PLC2 Venue | 2300 (EUR) | 27 | Register |

## United States Maryland- Columbia

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 1/15/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2700 (USD) | 27 | Register |
| **Designing with VHDL** | | | | | |
| 2/12/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-3 (BLT version)** | | | | | |
| 2/26/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2700 (USD) | 27 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 3/4/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 1800 (USD) | 18 | Register |
| **Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 3/6/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 1000 (USD) | 10 | Register |
| **DSP Design Using System Generator** | | | | | |
| 3/7/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2000 (USD) | 20 | Register |
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 3/12/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 3000 (USD) | 30 | Register |
| **Vivado Boot Camp Phase-1 (BLT version)** | | | | | |
| 3/26/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 5/7/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2700 (USD) | 27 | Register |
| **Designing with VHDL** | | | | | |
| 5/29/2019 | 8830 Stanford Boulevard #100 Columbia | USA, MD, Columbia - University of Phoenix Campus | 2700 (USD) | 27 | Register |

## United States Indiana- Fishers

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Classroom - Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 1/23/2019 | 11451 Overlook Fishers | USA, IN, Fishers - VAI Logic Headquarters | 1600 (USD) | 16 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 1/24/2019 | 11451 Overlook Fishers | USA, IN, Fishers - VAI Logic Headquarters | 1600 (USD) | 16 | Register |

# South Korea - Seoul

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 12/10/2018 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 500 (USD) | 6 | Register |
| **How to Design a High-Speed Memory Interface** | | | | | |
| 12/12/2018 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 500 (USD) | 6 | Register |
| **Embedded Systems Design** | | | | | |
| 12/17/2018 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 500 (USD) | 6 | Register |
| **Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 12/19/2018 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 500 (USD) | 6 | Register |
| **Classroom - Designing with Verilog** | | | | | |
| 1/2/2019 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 650 (USD) | 6 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 2** | | | | | |
| 1/7/2019 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 550 (USD) | 6 | Register |
| **Classroom - Designing with Ethernet MAC Controllers** | | | | | |
| 1/9/2019 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 550 (USD) | 6 | Register |
| **Classroom - Zynq SoC System Architecture** | | | | | |
| 12/17/2018 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 550 (USD) | 6 | Register |
| **Classroom - Embedded Design with PetaLinux Tools** | | | | | |
| 1/16/2019 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 650 (USD) | 9 | Register |
| **Classroom - C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 1/21/2019 | #B820, Tera tower 2, 201 Songpa-daero, Songpa-gu Seoul | KOR, Seoul - Wedu Office | 550 (USD) | 6 | Register |

# Japan - Tokyo

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Essentials of FPGA Design** | | | | | |
| 12/13/2018 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 800 (JPY) | 8 | Register |
| **Embedded Systems Software Design** | | | | | |
| 12/19/2018 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Advanced Features and Techniques of Embedded Systems Software Design** | | | | | |
| 12/21/2018 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 800 (JPY) | 4 | Register |
| **Essentials of FPGA Design (HDLab version)** | | | | | |
| 1/10/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 90808 (JPY) | 8 | Register |
| **Classroom - UltraFast Design Methodology** | | | | | |
| 1/16/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 4 | Register |
| **Classroom - Designing an Integrated PCI Express System** | | | | | |
| 1/17/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Classroom - Zynq SoC System Architecture** | | | | | |
| 1/22/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Debugging Techniques Using the Vivado Logic Analyzer (HDLab version)** | | | | | |
| 1/31/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 90808 (JPY) | 8 | Register |
| **Essentials of FPGA Design (HDLab version)** | | | | | |
| 2/7/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 90808 (JPY) | 8 | Register |
| **Classroom - Xilinx Partial Reconfiguration Tools & Techniques** | | | | | |
| 2/13/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 4 | Register |
| **Classroom - C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 2/14/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Vivado Design Suite Tool Flow (HDLab version)** | | | | | |
| 2/20/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 90808 (JPY) | 4 | Register |
| **Classroom - Embedded Systems Design** | | | | | |
| 2/21/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Classroom - Advanced Features and Techniques of Embedded Systems Design** | | | | | |
| 2/26/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Classroom - Zynq SoC System Architecture** | | | | | |
| 3/5/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Essentials of FPGA Design (HDLab version)** | | | | | |
| 3/7/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 90808 (JPY) | 8 | Register |
| **Debugging Techniques Using the Vivado Logic Analyzer (HDLab version)** | | | | | |
| 3/19/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 90808 (JPY) | 8 | Register |
| **Classroom - Embedded Systems Software Design** | | | | | |
| 3/27/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |
| **Classroom - Advanced Features and Techniques of Embedded Systems Software Design** | | | | | |
| 3/29/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 800 (JPY) | 4 | Register |
| **Classroom - SDSoC Development Environment and Methodology** | | | | | |
| 2/12/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 800 (JPY) | 4 | Register |
| **Classroom - Advanced SDSoC Development Environment and Methodology** | | | | | |
| 2/13/2019 | Art Village Osaki Central Tower 4F 1-2-2, Osaki, Shinagawa-ku Tokyo | JPN, Tokyo - Xilinx Japan Office | 1600 (JPY) | 8 | Register |

## United States California- San Jose

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Developing with Embedded Linux (Doulos version)** | | | | | |
| 12/10/2018 | 2100 Logic Drive San Jose | USA, CA, San Jose - Xilinx Learning Center | 3100 (USD) | 31 | Register |
| **UVM Adopter Class (Doulos course)** | | | | | |
| 12/10/2018 | 2100 Logic Drive San Jose | USA, CA, San Jose - Xilinx Learning Center | 3600 (USD) | 36 | Register |

## United States California- San Diego

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing with Xilinx Serial Transceivers** | | | | | |
| 12/19/2018 | 10815 Rancho Bernado Rd San Diego | USA, CA, San Diego - Xilinx San Diego Office | 1600 (USD) | 16 | Register |
| **Classroom - Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 12/17/2018 | 10815 Rancho Bernado Rd San Diego | USA, CA, San Diego - Xilinx San Diego Office | 1600 (USD) | 16 | Register |

## United States Virginia- Sterling

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 1/15/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 2700 (USD) | 27 | Register |
| **Designing with VHDL** | | | | | |
| 2/12/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-3 (BLT version)** | | | | | |
| 2/26/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 2700 (USD) | 27 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 3/4/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 1800 (USD) | 18 | Register |
| **Essential DSP Implementation Techniques for Xilinx FPGAs** | | | | | |
| 3/6/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 1000 (USD) | 10 | Register |
| **Embedded Systems Hardware Design Boot Camp (BLT version)** | | | | | |
| 3/12/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 3000 (USD) | 30 | Register |
| **Vivado Boot Camp Phase-1 (BLT version)** | | | | | |
| 3/26/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 2700 (USD) | 27 | Register |
| **Vivado Boot Camp Phase-2 (BLT version)** | | | | | |
| 5/7/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 2700 (USD) | 27 | Register |
| **Designing with VHDL** | | | | | |
| 5/29/2019 | 22685 Holiday Park Drive, Suite 60 Sterling | USA, VA, Sterling - Executive Conference & Training Center | 2700 (USD) | 27 | Register |

## Online

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 1/10/2019 | Online | | 1600 (USD) | 16 | Register |
| **Zynq-7000 All Programmable SoC System Architecture** | | | | | |
| 1/8/2019 | Online | | 1600 (USD) | 16 | Register |
| **Designing with System Verilog** | | | | | |
| 2/4/2019 | Online | | 2400 (USD) | 24 | Register |
| **Virtual - Zynq UltraScale+ MPSoC for the Software Developer** | | | | | |
| 2/7/2019 | Online | | 1600 (USD) | 16 | Register |

## United States Minnesota- Orono

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 3** | | | | | |
| 12/10/2018 | 2500 Shadywood Rd Orono | USA, MN, Orono -- MAPS Training Center | 1600 (USD) | 16 | Register |
| **STA, XDC, and Advanced Tools and Techniques of Vivado Design Suite-custom (MAPS)** | | | | | |
| 12/12/2018 | 2500 Shadywood Rd Orono | USA, MN, Orono -- MAPS Training Center | 2700 (USD) | 27 | Register |
| **Classroom - Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 2/4/2019 | 2500 Shadywood Rd Orono | USA, MN, Orono -- MAPS Training Center | 1600 (USD) | 16 | Register |
| **Classroom - C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 2/7/2019 | 2500 Shadywood Rd Orono | USA, MN, Orono -- MAPS Training Center | 1600 (USD) | 16 | Register |
| **Classroom - Embedded Design with PetaLinux Tools** | | | | | |
| 12/27/2018 | 2500 Shadywood Rd Orono | USA, MN, Orono -- MAPS Training Center | 1600 (USD) | 16 | Register |

## Canada British Columbia- Coquitlam

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Embedded System Design for the Zynq UltraScale+ MPSoC (combined course)** | | | | | |
| 2/25/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **Embedded Design with PetaLinux Tools** | | | | | |
| 2/28/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 3/12/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 1/21/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **SDSoC Development Environment and Methodology** | | | | | |
| 1/23/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 800 (USD) | 8 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 1/24/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **SystemVerilog for Verification** | | | | | |
| 1/14/2019 | TBD Coquitlam | CAN, BC, Coquitlam - TBD Hardent Venue | 2800 (USD) | 28 | Register |

## United States Alabama- Huntsville

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 1/15/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **SDSoC Development Environment and Methodology** | | | | | |
| 4/10/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 800 (USD) | 8 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 4/11/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 4/8/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Embedded System Design for the Zynq UltraScale+ MPSoC (combined course)** | | | | | |
| 2/18/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **Embedded Design with PetaLinux Tools** | | | | | |
| 2/21/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 4/24/2019 | TBD Huntsville | USA, AL, Huntsville - TBD Hardent Venue | 1800 (USD) | 18 | Register |

## Canada Ontario- Ottawa

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **SystemVerilog for Verification** | | | | | |
| 2/25/2019 | 15 Fitzgerald Road Ottawa | CAN, ONT, Ottawa -- Avnet Office | 2800 (USD) | 28 | Register |
| **Developing AWS F1 Applications Using the SDAccel Environment Course - Classroom** | | | | | |
| 12/11/2018 | 15 Fitzgerald Road Ottawa | CAN, ONT, Ottawa -- Avnet Office | 900 (USD) | 9 | Register |

## Japan - Yokohama Shi, Kanagawa

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Understand IP Management with Vivado Design Suite (HDLab version)** | | | | | |
| 12/18/2018 | 3-17-6 Shin-Yokohama Kohhoku-ku Yokohama Shi, Kanagawa | JPN, Yokohama Shi, Kanagawa - HD Lab, Inc. | 45404 (JPY) | 4 | Register |
| **Vivado Design Suite For Large Design (HDLab version)** | | | | | |
| 12/19/2018 | 3-17-6 Shin-Yokohama Kohhoku-ku Yokohama Shi, Kanagawa | JPN, Yokohama Shi, Kanagawa - HD Lab, Inc. | 45404 (JPY) | 4 | Register |

## United States Wisconsin- Milwaukee

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 2/7/2019 | Milwaukee, WI Milwaukee | USA, WI, Milwaukee - MAPS Venue | 1600 (USD) | 16 | Register |

## United States Missouri- St. Louis

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Embedded Design with PetaLinux Tools** | | | | | |
| 12/10/2018 | St. Louis St. Louis | USA, MO, St. Louis - MAPS Venue 2 | 1600 (USD) | 16 | Register |

## United States Iowa- Cedar Rapids

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 12/17/2018 | Cedar Rapids, IA Cedar Rapids | USA, IA, Cedar Rapids - MAPS Venue | 1600 (USD) | 16 | Register |
| **STA, XDC, and Advanced Tools and Techniques of Vivado Design Suite-custom (MAPS)** | | | | | |
| 1/7/2019 | Cedar Rapids, IA Cedar Rapids | USA, IA, Cedar Rapids - MAPS Venue | 2700 (USD) | 27 | Register |
| **Zynq UltraScale+ MPSoC for the Software Developer** | | | | | |
| 1/10/2019 | Cedar Rapids, IA Cedar Rapids | USA, IA, Cedar Rapids - MAPS Venue | 1600 (USD) | 16 | Register |

## United States Illinois- Schaumburg

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 1/21/2019 | 475 N. Martingale Rd. Schaumburg | USA, IL, Schaumburg - Xilinx Office | 1600 (USD) | 16 | Register |

## United States Kansas- Olathe

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Classroom - Designing with VHDL** | | | | | |
| 2/4/2019 | Olathe, KS Olathe | USA, KS, Olathe - MAPS Venue | 2400 (USD) | 24 | Register |

## United States Kansas- Wichita

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing with the UltraScale and UltraScale+ Architectures** | | | | | |
| 1/17/2019 | Wichita, KS Wichita | USA, KS, Wichita - MAPS Venue | 1600 (USD) | 16 | Register |

## United States Wisconsin- Madison

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **STA, XDC, and Advanced Tools and Techniques of Vivado Design Suite-custom (MAPS)** | | | | | |
| 12/19/2018 | Madison, WI Madison | USA, WI, Madison - MAPS Venue | 2700 (USD) | 27 | Register |
| **Designing FPGAs Using the Vivado Design Suite 1** | | | | | |
| 12/17/2018 | Madison, WI Madison | USA, WI, Madison - MAPS Venue | 1600 (USD) | 16 | Register |

## United States NorthCarolina- Raleigh

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 2/26/2019 | TBD Raleigh | USA, NC, Raleigh - TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 4/11/2019 | TBD Raleigh | USA, NC, Raleigh - TBD Hardent Venue | 1800 (USD) | 18 | Register |

## United States Utah- Salt Lake City

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 3/25/2019 | Salt Lake City | USA, UT, Salt Lake City -- TBD Faster Technology Venue | 1600 (USD) | 16 | Register |
| **Zynq UltraScale+ MPSoC for the System Architect** | | | | | |
| 2/13/2019 | Salt Lake City | USA, UT, Salt Lake City -- TBD Faster Technology Venue | 1600 (USD) | 16 | Register |

# United States Massachusetts- Burlington

| Date | Location | Facility | Price | TC | Reg. URL |
|---|---|---|---|---|---|
| **Vivado Design Suite Advanced XDC and Static Timing Analysis with Design Methodology (combined course)** | | | | | |
| 1/28/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **Embedded System Design for the Zynq UltraScale+ MPSoC (combined course)** | | | | | |
| 3/11/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 2400 (USD) | 24 | Register |
| **C-based design: High-Level Synthesis with Vivado HLx Tool** | | | | | |
| 3/18/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **SDSoC Development Environment and Methodology** | | | | | |
| 3/20/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 800 (USD) | 8 | Register |
| **Advanced SDSoC Development Environment and Methodology** | | | | | |
| 3/21/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **SystemVerilog for Verification** | | | | | |
| 2/11/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 2800 (USD) | 28 | Register |
| **Introduction to Universal Verification Methodology (UVM)** | | | | | |
| 3/18/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 2800 (USD) | 28 | Register |
| **Embedded Design with PetaLinux Tools** | | | | | |
| 3/14/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Advanced Universal Verification Methodology (UVM) (Hardent version)** | | | | | |
| 2/19/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 3000 (USD) | 30 | Register |
| **Xilinx Partial Reconfiguration Tools & Techniques** | | | | | |
| 2/26/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 1600 (USD) | 16 | Register |
| **Classroom - Designing with the Zynq UltraScale+ RFSoC** | | | | | |
| 2/12/2019 | TBD Burlington | USA, MA, Burlington -- TBD Hardent Venue | 1800 (USD) | 18 | Register |

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